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August 13, 2007

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Customer No. 66785

Re: Applicants: Jian Chen et al.
Title: Read and Erase Verify Methods and Circuits Suitable for Low Voltage Non-Volatile Memories
Application No.: 10/552,948 Filing Date: September 11, 2006
Examiner: Yoha, Connie C. Group Art Unit: 2827
Docket No.: SNDK.284US1 Conf. No.: 6753

Dear Sir:

Transmitted herewith are the following documents in the above-identified application:

- (1) This Transmittal Letter; and
- (2) Power of Attorney by Assignee of Entire Interest (2 pages).

☒ No additional fee is required.

FILED VIA EFS

Respectfully submitted,

Gerald P. Parsons
Reg. No. 24,486